Electronic Version
Stylesheet Version v1.1.1

SWITCHED CAPACITOR CIRCUIT CAPABLE OF MINIMIZING CLOCK FEEDTHROUGH EFFECT AND HAVING LOW PHASE NOISE AND METHOD THEREOF

Abstract

A switched capacitor circuit includes a capacitor; a switch element for selectively coupling a first node to a second node according to a control signal, wherein the first node is coupled to the capacitor; and a charge circuit coupled to the first node for coupling the first node to a third node and for controlling a first voltage difference across the first switch element in the off-state to be greater than a charge voltage. By ensuring the charge voltage is large enough to minimize a parasitic capacitance of the switch element, the clock feedthrough effect is eliminated, the locking period of the VCO is shortened, and the phase noise of the VCO is minimized.